Integrated Receiver Simplifies the Analog Side of Digital Predistortion

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> IC design and manufacturing expertise is combined with advanced circuit design, layout and packaging techniques in this high performance digital-output receiver module

Dramatic advances in digital processing power have created an increased demand for high performance analog signal processing products. Cellular networks today provide significant data and video in addition to traditional voice, at faster rates than ever before. This has led to new modulation techniques and new air interface standards that rely on complex digital techniques. While digital techniques enable systems to run faster, consume less power, using smaller package sizes and at higher reliability with each generation, these systems place new demands on the RF and analog signal acquisition portion of the system.

The complex modulation and wide bandwidth of base station transmitters result in higher crest factors for the power amplifier (PA). To meet the more stringent requirements in the presence of higher crest factors, the power amplifier is typically oversized to enable operation in the linear region. Without digital correction, the PA efficiency can be on the order of 10%, meaning 200 W capability is required to for a 20 W PA. The PA is the largest consumer of electrical power in a base station and, therefore, a significant factor in the operating expense for the cellular service provider. To improve PA efficiency, digital techniques are used for crest factor reduction (CFR) and digital predistortion (DPD).

While an amplifier is most efficient when driven into saturation, it becomes highly nonlinear. Complex digital modulation requires extremely high linearity from the PA which consequently means that it must be driven well below saturation. Operating the PA just below saturation offers good efficiency if there is a way to compensate for the inherent nonlinearity of the amplifier. Digital predistortion has emerged as the preferred method of PA linearization.

DPD is a feedback technique where the output of the PA is sampled and converted to digital data. A distortion-free transmit signal, stored in a FIFO, is compared to the feedback signal, creating an inverse of the transfer function. This is summed with the transmit data after CFR to reduce the nonlinearity of the PA output. An adaptive algorithm or lookup table—or combination of these methods—may be used to produce the compensating digital signal. Technical details of DPD are beyond the scope of this article. Here we will focus on the analog requirements for the receiver that samples the PA output.

DPD Receiver Requirements

The receiver is the signal chain that converts from RF to digital (see Figure 1). Key design requirements are the input frequency
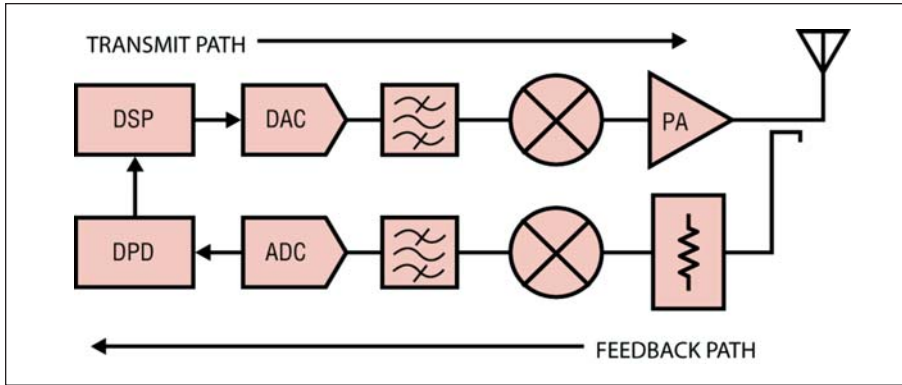
Figure 1 · Digital predistortion signal chain.

range and power level, the intermediate frequency, and the bandwidth to be digitized. Some of these are derived directly from the PA specifications and some are optimized during design.

The baseband transmit signal is upconverted to the carrier frequency and is defined in frequency by the air interface standard: WCDMA, TD-SCDMA, CDMA2000, LTE, etc. Therefore the output spectrum to be sampled exists within a well-defined range of frequencies, i.e., the desired channel. Since the purpose of the DPD loop is to measure the PA transfer function, it is not necessary to separate the carriers in multicarrier systems or demodulate the digital data. It is only necessary to capture information regarding the entire desired channel.

PA nonlinearity produces odd order intermodulation products which constitute spectral regrowth in the adjacent and alternate channels. By definition, third-order products appear at $2f_a + f_b$, $2f_b + f_a$, $2f_a - f_b$ and $2f_b - f_a$, where f_a and f_b are the frequencies of two signals within the desired channel that cause intermodulation distortion outside the channel. For a modulated channel, third-order products appear within a range of three times the bandwidth of the desired channel (see Figure 2). Likewise, fifth-order products appear within a range of five times the bandwidth and seventh-order products within seven times the bandwidth. Therefore, the DPD receiver must acquire a multiple of the transmit bandwidth, equivalent to the order of the intermodulation products being linearized.
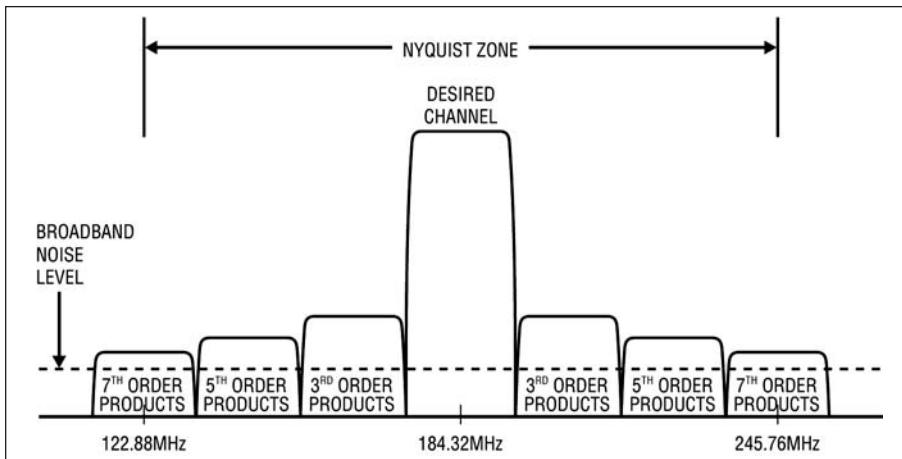
The trend in current development

is to mix the desired channel to an intermediate frequency (IF) and capture the full bandwidth of all the intermodulation products. The exact IF is chosen to ease filtering and avoid other frequencies that are already fixed based on specification requirements. The sample rate is similarly chosen as a multiple of the digital modulation chip rate, for example, 3.84 MHz in WCDMA. Finally, the Nyquist theorem dictates that the sample rate must be at least twice the sampled bandwidth. Although many configurations are acceptable, one that meets these constraints is an IF of 184.32 MHz, an ADC sample rate of 245.76 MHz and a bandwidth of 122.88 MHz.

In the case of a 20 W PA, the average output power is 43 dBm and the peak to average ratio (PAR) is about 15 dBm. To set the average input power to the mixer of the receive chain at –15 dBm, the combination of the coupler and attenuator insertion losses needs to be 58 dB (refer to Figure 1). The in-band noise of the PA is specified by the WCDMA standard at a maximum of –13 dBm/MHz (–73 dBm/Hz). Therefore, the combination of the coupler and attenuation (–58 dB) and the PA noise limit (–13 dBm/MHz) yields a receiver sensitivity level that must be below –71 dBm/MHz (–131 dBm/Hz). For sufficient margin, a number at least 6 dB to 10 dB better than this is desirable. This sets the frequency plan, power level and sensitivity requirements for the DPD receiver.

Integrated DPD Receiver

Once the system requirements are defined, the task turns to the circuit implementation using a mixer, IF amplifier, ADC, passive filtering, matching networks and supply bypassing. While calculations and simulations are helpful, there is no substitute for evaluation of real hardware, which generally leads to multiple printed circuit board (PCB) iterations. However, a new class of inte-

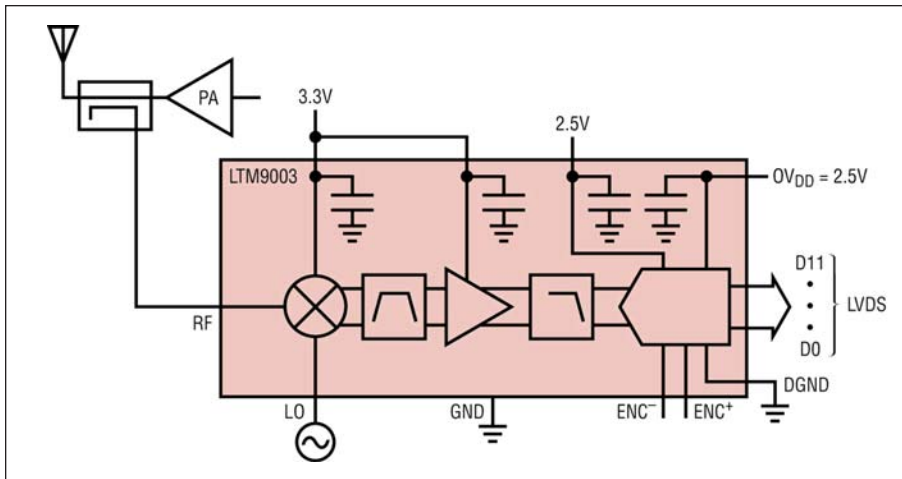Figure 2 · Odd-order intermodulation products.

Figure 3 · LTM9003 integrated digital predistortion receiver.

grated receivers based on system in package (SiP) technology greatly simplifies this task. The LTM9003 digital predistortion uModule® receiver is a fully integrated DPD receiver—essentially RF-to-bits.

The μModule technology pioneered by Linear Technology utilizes a thin, multi-layer laminate substrate made of BT (bismaleimide triazine) material. The multi-layer substrate allows the design of complex circuits using RF components, standard wire-bonded IC die and traditional passive components. The circuit is encapsulated with standard IC package molding compound and the land grid array (LGA) pad arrangement is consistent with current surface mount assembly methods. The result is a subsystem that looks and feels like a traditional IC, is thoroughly tested, ensuring the high reliability of an IC, yet integrates components from different semiconductor process technologies along with passives in a compact footprint smaller than traditional implementations.

The LTM9003 consists of a high linearity active mixer, an IF amplifier, an L-C bandpass filter and a high-speed analog-to-digital converter (ADC) (see Figure 3). The wire-bonded bare die assembly ensures that the overall form factor is highly compact, but also allows the reference

and supply bypass capacitors to be placed closer to the die than possible with traditional packaging. This reduces the potential for noise to degrade the fidelity of the ADC. This idea extends to the high frequency layout techniques used throughout the receiver chain of the LTM9003.

The integration eliminates many challenges of driving high-speed ADCs. For example, linear circuit analysis cannot account for the current pulses resulting from the sample-and-hold switching action of the ADC, so traditional circuit layout requires multiple iterations to define an input network that absorbs these pulses, is absorptive out of band, yet works seamlessly with the preceding amplifier. The IF amplifier must also be capable of driving this network without adding distortion. Solving these challenges may be the greatest hidden attribute of the LTM9003 μModule receiver.

The passive bandpass filter is a 3rd order filter with an extremely flat passband. Within the center 25 MHz of the band it exhibits less than 0.1 dB ripple, and over the entire 122 MHz bandwidth the passband ripple is only 0.5 dB. The 3rd order configuration ensures that the shoulders of the frequency response are monotonic which is important for many DPD algorithms.

The overall performance of the LTM9003 greatly exceeds the system requirements described above. With a single tone at –2.5 dBm, which is equivalent to –1 dBFS at the ADC, the signal to noise ratio (SNR) is typically –145 dBm/Hz. This figure is well below the target value of –131 dBm/Hz defined by the WCDMA standard. The worst case harmonics are 60 dBc. The IIP3 figure of 25.7 dBm means that the LTM9003 could support an ACPR of 87 dBc if the PA were linear enough. Relative to the system requirements and the capability of the best power amplifiers available, the LTM9003 greatly exceeds the requirements. The entire chain consumes about 1.5 W from a 3.3 V and a 2.5 V supply, yet requires a circuit board area of only 11.25 × 15 mm.

Flexibility Without Compromise

The μModule technology also offers an unexpected level of flexibility. Traditional highly integrated circuits may offer flexibility in terms of programmable modes or selectable features, but this adds complexity and often some loss of performance. By changing the values of the passive components or substituting ICs that are optimized as a group, the LTM9003 is available in specific versions, with no loss of performance or increased complexity.

For example, the LTM9003-AA utilizes a low power, silicon germanium active mixer operating from a 3.3 V supply. The $2 \times RF – 2 \times LO$ product gives a 60 dBc second harmonic, which is the worst spur in the spectrum. This can be improved at the expense of power consumption by replacing the mixer with a similar 5 V part. The second harmonic is then improved by 6 dB in the LTM9003-AB. Similarly, the sample rate can be reduced by substituting a 210 Msps ADC which consumes less power and the L-C filter values can be changed to realize a 100 MHz bandwidth filter in yet another version of the

LTM9003. The filter will be optimized for passband flatness and optimal signal chain performance without the use of lossy switches. Prefer a different IF? This can be provided by changing the values of a few passive components.

Green, Small and Easy

The benefits of using the LTM9003 for PA linearization occur at several levels. At a high level, DPD allows you to run the PA with less back-off. The result is that the PA is more efficient and therefore consumes less power for the same output power level. As discussed earlier, the PA is the most significant factor in electrical power consumption for the base station. If your company has a "green initiative" then DPD is your contribution. Regardless, using less electricity reduces operating expenses for the service provider and makes your product more competitive.

At the board level, the µModule packaging integrates all of the key components into a small area including the passives for filtering and decoupling. This saves board space, simplifies layout and makes room for other features that further increase the value of the product.

At the engineering level, the LTM9003 saves time. Filter design and component matching can be done in simulation but in most cases iteration is required to get it right. Designing a filter that is not disturbed by the switching action of the ADC sample and hold circuitry is especially challenging. Even something as routine as placing capacitors for supply decoupling affects overall performance and can cause board layout revisions. These tasks can easily consume months of engineering time debugging each revision and evaluating the changes. In this area of design, the LTM9003 provides a direct savings of time and resources.

Conclusion

Digital processing power offers several methods to improve the efficiency of base station power amplifiers. Improvements in PA efficiency lead to significant reduction in the operating expense for cellular service providers. Digital predistortion of the PA requires a low noise, high-speed receiver chain based on high performance analog components. In most cases, working with a high performance analog component adds complexity and requires more engineering time and resources. However, advances in integration such as the LTM9003 greatly simplify this task and allow the designer to focus on improving the digital algorithms.

Author Information

Todd Nelson is currently Signal Chain Development Manager for Linear Technology's signal chain µModule products. Prior to that, Todd was product marketing manager for Linear's mixed signal products with responsibility for all data converters, interface transceivers, system monitoring products, Hot Swap™ controllers and powered Ethernet devices. He also held various marketing and applications positions at National Semiconductor prior to joining Linear Technology in 1995. Todd earned his Bachelor's degree in engineering from Kettering University, and his Masters in engineering management from Santa Clara University. He has published numerous technical articles and papers and participated on various standards committees. He can be reached at tnelson@linear.com

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